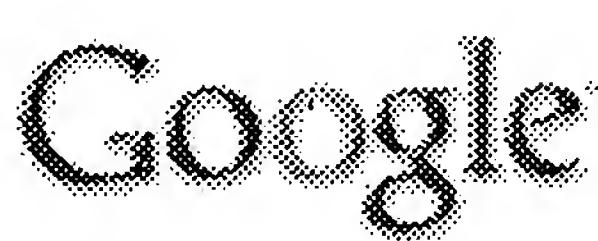


Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	"5978584".pn. and fpga	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/06 14:45
L2	340	beck.in. and ice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/06 14:45
L3	5	beck.in. and (master adj processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/06 14:45
S1	0	703/28.ccls. and ((lock\$step synchron\$8) same boot)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/06 08:59
S2	8	703/28.ccls. and ((lock\$step synchron\$8) and boot)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/05 14:11
S3	31	("4590581" "4635218" "4691316" "4744084" "5036473" "5068852" "5136590" "5146460" "5226047" "5325365" "5353243" "5369593" "5448496" "5452231" "5475624" "5528752" "5539901" "5546562" "5574892" "5612891" "5625580" "5630102" "5657241" "5661662" "5748875" "5771370" "5838948" "5946472" "6009256").PN. OR ("6202044").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:17
S4	11	S3 and boot	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:25
S5	5	703/28.ccls. and (pod and boot)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:25
S6	2	S5 not S2	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:25

S7	16	("4272760" "5313618" "5375228" "5467200" "5488688" "5752077" "5758059" "5872954" "5898862").PN. OR ("6230119").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:26
S8	2	S7 and boot	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:55
S9	0	703/28.ccls. and (concurrency and spin\$lock)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:55
S10	2	703/28.ccls. and (concurrency)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:57
S11	1	tzori.in. and 703/28.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 14:57
S12	1	"5748875".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/05 16:44
S13	9	(716/4.ccls. 716/5.ccls. 716/6.ccls. 716/18.ccls. 703/28.ccls.) and (lock\$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/05 16:50
S14	6	("5771370" "5805867" "5978584" "6014512" "6356862").PN. OR ("6718294").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/06 10:00
S17	1	nemecek and (lock\$step) and ice	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/06 10:00
S18	24	nemecek.in. and ice	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/06 10:01
S19	2	nemecek.in. and (microcontroller)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/06 10:02
S20	1114	(cypress.as. and semiconductor. as.)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/06 10:02
S21	0	S20 and ice	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/06 10:02
S22	4	S20 and emulator	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/06 10:03

S23	4	S20 and emulator	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/06 10:04
S24	0	S20 and nemecek.in.	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/06 10:05
S25	1	(nemecek.in. and roe.in.)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/06 10:08
S26	27	S20 and boot	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/06 10:09
S27	1	S20 and boot.clm.	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/06 10:59

**Web**Results 1 - 10 of about 384 for **sparc fpga emulated advantages**. (0.29 seconds)[A Reconfigurable Logic Machine for Fast Event-Driven Simulation](#)

... This system has a number of **advantages**: Logic (in the **FPGA** array) can be ...

The netlist portion of the design is **emulated** in the **FPGA** array. ...

www.bearcave.com/dac_paper/dac_paper_final.html - 22k - Cached - Similar pages

[\[PDF\] Analysis of SEU effects in a pipelined processor](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

... behavior of the **emulated** system. A major advantage of the adopted fault ...

with the **emulated** system. Figure 1: The **FPGA**-based fault injection flow ...

www.cercom.polito.it/Publication/Pdf/152.pdf - Similar pages

[\[PDF\] Virtual Wires: Overcoming Pin Limitations in **FPGA**-based Logic ...](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

... the logic design to be **emulated**, target **FPGA** device char- ... running times

on a **SPARC** 2 workstation were usually 1 to. 15 minutes for each stage. ...

www.ecs.umass.edu/ece/tessier/courses/697ff/ps3/fccm93.pdf - Similar pages

[\[PPT\] Rapid Prototyping Using Field Programmable Devices](#)

File Format: Microsoft Powerpoint 97 - [View as HTML](#)

... **Advantages** and Disadvantages of **FPGA**. Fast turnaround. ... Control HW/SW to support operation of the **emulated** design as a hardware component operating ...

nthucad.cs.nthu.edu.tw/AllenWu/cs6133_99/5_prototype.ppt - Similar pages

[Citations: Virtual Wires: Overcoming pin limitations in **FPGA**-based ...](#)

... Virtual wire technology [2], 5] 11] takes advantage of the high **FPGA** speed,

... each **FPGA** pin (physical wire) to a single **emulated** signal (logical wire) ...

citeseer.csail.mit.edu/context/46431/527559 - 66k - Cached - Similar pages

[\[PDF\] Emulation of the Sparcle microprocessor with the MIT Virtual Wires ...](#)

File Format: PDF/Adobe Acrobat

... plementation of a modified **Sparc** microprocessor. Vir- ... description of the

system to be **emulated**. and produces programming information for the **FPGA** ...

ieeexplore.ieee.org/iel2/949/7612/00315594.pdf?arnumber=315594 - Similar pages

[\[PDF\] A Prototyping System for Verification and Evaluation in Hardware ...](#)

File Format: PDF/Adobe Acrobat

... application specific coprocessor, which is **emulated** by ... Communication.

Between the **SPARC**. and the **FPGA** Board. Currently, processor and coprocessor ...

doi.ieeecomputersociety.org/10.1109/IWRSP.1995.518571 - Similar pages

[RPM: A Rapid Prototyping Engine for Multiprocessor Systems](#)

... Eight identical boards, each with one **Sparc** processor, are connected to a ...

other **FPGA**-based emulators where circuits are **emulated** by **FPGA** arrays. ...

doi.ieeecomputersociety.org/10.1109/2.347997 - Similar pages

[\[PS\] A Reconfigurable Compute Engine for Real-Time Vision Automata ...](#)

File Format: Adobe PostScript - [View as Text](#)

... of very coarse grain applicationspecific **FPGA** called the Field-Programmable
... of the **emulated** hardware since it is optimized at the operator level. ...
www-clips.imag.fr/mrim/ georges.quenot/articles/fccm94.ps - [Similar pages](#)

[EP692124 Massachusetts european software patent - Virtual wires ...](#)
... compiler programs each **FPGA** chip to emulate a partition of an **emulated** ...
Thus, any existing **FPGA**-based logic emulation system can take advantage of ...
gauss.ffii.org/PatentView/EP692124 - 64k - [Cached](#) - [Similar pages](#)

Google ►

Result Page: 1 2 3 4 5 6 7 8 9 10 [Next](#)

Free! Google Desktop Search: Search your own computer. [Download now.](#)

Find: emails ~ files ~ chats ~ web history ~ media ~ PDF

sparc fpga emulated advantages

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2005 Google



Web

Results 11 - 20 of about 509 for **sparc fpga emulated**. (0.05 seconds)

[PDF] [Emulation of the Sparcle microprocessor with the MIT Virtual Wires ...](#)

File Format: PDF/Adobe Acrobat

... plementation of a modified **Sparc** microprocessor. Vir- ... description of the system to be **emulated**. and produces programming information for the **FPGA** ...
ieeexplore.ieee.org/iel2/949/7612/00315594.pdf?arnumber=315594 - [Similar pages](#)

[RPM: A Rapid Prototyping Engine for Multiprocessor Systems](#)

... Eight identical boards, each with one **Sparc** processor, are connected to a ... other **FPGA**-based emulators where circuits are **emulated** by **FPGA** arrays. ...
doi.ieeecomputersociety.org/10.1109/2.347997 - [Similar pages](#)

[PDF] [A Prototyping System for Verification and Evaluation in Hardware ...](#)

File Format: PDF/Adobe Acrobat

... application specific coprocessor, which is **emulated** by ... Communication. Between the **SPARC**. and the **FPGA** Board. Currently, processor and coprocessor ...
doi.ieeecomputersociety.org/10.1109/IWRSP.1995.518571 - [Similar pages](#)

[Citations: Virtual Wires: Overcoming pin limitations in **FPGA**-based ...](#)

... dedicate each **FPGA** pin (physical wire) to a single **emulated** signal (logical wire)

... Emulation of a **Sparc** Microprocessor with the **MIT**.. - Dahl, Babb. ...

citeseer.csail.mit.edu/context/46431/527559 - 66k - [Cached](#) - [Similar pages](#)

[Virtual Wires' Overcoming Pin Limitations in **FPGA**-based Logic ...](#)

... because they dedicate each **FPGA** pin (physical wire) to a single **emulated** signal (logical. ... 1.3: Emulation of a **Sparc** Microprocessor with the **MIT**. ...
citeseer.csail.mit.edu/527559.html - 21k - [Cached](#) - [Similar pages](#)

[PS] [A Prototyping System for Verification and Evaluation in Hardware ...](#)

File Format: Adobe PostScript - [View as Text](#)

... and an application specific coprocessor, which is **emulated** by XILINX FPGAs.

... 4.2 Communication Between the **SPARC**. and the **FPGA** Board Currently, ...

www.ida.ing.tu-bs.de/research/publications/ps/BEK+95:ProtoSysteVerifEvalu.ps - [Similar pages](#)

[EP692124 Massachusetts european software patent - Virtual wires ...](#)

... compiler programs each **FPGA** chip to emulate a partition of an **emulated** circuit

... on a **SPARC** 2 workstation were usually 1 to 15 minutes for each stage. ...

gauss.ffii.org/PatentView/EP692124 - 64k - [Cached](#) - [Similar pages](#)

[PDF] [LEON Open-Source Processor](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

... Full **SPARC** V8 ISA - reuse of standard **SPARC** tools ... Low-cost LEON PCI **FPGA** development board available with. XC2V3000, 64 Mbyte SDRAM, Flash, SRAM, ...
www.embedded-kernel-track.org/2004/leonpres-long.pdf - [Similar pages](#)

[Transit Note #18 MBTA: Thoughts on Construction](#)

... We can always deal with **emulated** any other memory configurations ... seems optimal to start with some form of Field Programmable Gate Arrays (**FPGA**'s). ...

www.cs.caltech.edu/research/ic/transit/tn18/tn18.html - 24k - [Cached](#) - [Similar pages](#)

[PDF] [Research Projects IC and System Design and Test](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

... Processors (SP) and a Sparc V8 compliant host CPU. Power Dissipation in Microelec-

... is either implemented in an **FPGA** or **emulated** on a differ- ...

www.iis.ee.ethz.ch/portrait/review/2003/12.Digital03.pdf - [Similar pages](#)

◀ Gooooooooooooogle ▶

Result Page: [Previous](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [Next](#)

[Search within results](#) | [Language Tools](#) | [Search Tips](#)

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2005 Google